UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,891	11/13/2003	Dong-Yang Lee	5649-1203	7749

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EXAMINER
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ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>11 July 2005</u>.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-12 and 16-24</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-12 and 16-24</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>25 April 2005</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All b)☐ Some * c)☐ None of:

      1.☒ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☒ Other: <u>Search history</u>.

DETAILED ACTION

1.   This action is responsive to the following communication filed on 7/11/05. Claims 13 – 15

have been canceled. Claims 1-12 and 16- 24 remain in this application.

Response to arguments

2.   Applicant's arguments filed on 4/25/05 with respect to claims 1, 7, and 16 have

been considered, but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

3.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 – 12 and 16 – 24 are rejected under 35 U.S.C. 102(b) as being

anticipated by Satagopan et al. U.S. Patent No. 6,571,325 – filed: Sep. 23, 1999.

Regarding independent claim 1, Figure 5 of Satagopan et al. discloses a

method of precharging a bank of memory cells (Fig. 3) in a semiconductor memory

device (Table 1 on Col. 11 line 50 – Col. 12 line 10), the method comprising: receiving a

command that includes an auto-precharge function to the semiconductor memory

device (Col. 12 lines 47 – 48); initiating a timer (570) in response to the received

command (Col. 12 lines 48 - 51); and automatically precharging the bank responsive to

the timer (570) reaches a predetermined value (Col. 12 lines 52 – 64).

Regarding dependent claim 2, Satagopan discloses wherein the received

command is associated with data stored in a specific row of the bank (Fig. 5 [560]), and

wherein the method further comprises resetting the timer (TABLE 1 on Col. 11) when

prior to the timer reaching the predetermined value a second command is received by

the semiconductor memory device (Col. 11 line 34 – Col.12 lines 22) that is associated

with additional data stored in the specific row of the bank.

Regarding dependent claim 3, Fig. 5 of Satagopan et al. further discloses

wherein the received command is associated with data stored in a specific row of the

bank (Fig. 1), and wherein the method further comprises precharging the bank when

prior to the timer reaching the predetermined value (Col. 12 lines 51 – 65) a second

command (Col. 12 lines 11 - 22) is received by the semiconductor memory device that

is associated with data stored in a different row of the bank (See Table 1 Col. 11 lines

64).

Regarding dependent claim 4, Fig. 5 of Satagopan discloses wherein the

received command is associated with data stored in a specific row of the bank (Fig. 1),

and wherein the specific row of the bank is left open for a period of time after an

operation associated with the command is completed (Col. 12 lines 51 – 65).

Regarding dependent claim 5, Fig. 5 of Satagopan discloses wherein the

received command is a first read command (Col. 10 lines 51 – 58) and wherein the

method further comprises performing a first read operation in response to the first read

command and performing a second read operation after completion of the first read

operation (Col. 10 line 59 – Col. 11 line 3) using a page mode operation (Col. 11 lines

10 – 24).

Regarding dependent claim 6, Satagopan et al. discloses the method further

comprising initiating a second timer in response to the received command and storing a

row address associated with the received command (See TABLE I on Col. 11 for

disclosing multiples timing constrain for receiving command and storing a row address

of Fig. 5 having multiple timers of Fig. 7[720]).

Regarding independent claim 7, Satagopan et al. discloses a semiconductor

memory device, comprising: a memory cell array arranged in rows and columns (Fig. 3

and 4); and a precharge control circuit (Fig. 7 Precharge FSM]) having at least one

timer Fig. 7 [720]) wherein the precharge control circuit (Fig. 7 Precharge FSM]) is

configured to issue a precharge control signal to the memory cell array responsive to

receipt of a command (TABLE 1 on Col. 11) that includes an auto-precharge function a

predetermined time after the command is received (Col. 12 lines 46 – 64).

Regarding dependent claim 8, Fig. 7 of Satagopan et al. discloses wherein the

precharge control circuit (Fig. 7 Precharge FSM]) issues an auto-precharge control

signal to the memory cell array responsive to the at least one timer (Fig. 7[720])

reaching the predetermined time (TABLE 1 on Col. 11 and Col. 12 lines 46 – 64)

Regarding dependent claim 9, Fig. 7 of Satagoban et al. further comprising a

storage device that stores the predetermined time (TABLE 1).

    Regarding dependent claim 10, Satagopan discloses wherein the

semiconductor memory device (Fig. 2) further comprises a second timer (Fig. 7 [720])

that measures a passage of the predetermined auto precharging time and a row

address storage register that is associated with second timer (TABLE 1 on Col. 11)

    Regarding dependent claim 11, Fig. 5 of Satagopan et al. further comprising a

row decoder (520) for decoding an externally received row address ([510]; see Col. 8

lines 18 – 35) and a command decoder (560) that activates an auto-precharge control

signal in response to the input of a command having the auto-precharge function (Col.

10 lines 43 – 58).

    Regarding dependent claim 12, Fig. 5 of Satagopan et al. discloses a method

of precharging a bank of memory cells (Fig. 3) in a semiconductor memory device, the

method comprising: receiving at the semiconductor memory device a read command

that includes an auto-precharge function (Col 11 lines 24)); starting a timer responsive

to receiving the received read command (TABLE 1 on Col. 11); performing a read

operation responsive to the received read command (Col. 11 lines 50 – 53); delaying

initiation of an auto-precharge operation called for by the auto-precharge function until

the timer reaches a predetermined time (Col. 12 lines 51 – 64).

    Regarding dependent claim 16, Fig. 2 of Satagopan et al. discloses a

semiconductor memory device comprising: a memory cell array disposed in rows and

column (Fig. 4); a row decoder for decoding (Fig. 5 [520]) an external received

commands Fig. 5 [510]) and activating an auto-precharge control signal (Fig. 5[560])

when a decoded command includes an auto-precharge function (Col. 10 lines 43 – 58);

and a precharge control circuit (Fig. 7 [Precharge FSM]) that includes at least one timer

(Fig. 7[720]) that is reset in response to the auto-precharge control signal that initiates

precharging of at least a part of the memory cell array when the at least one timer

reaches a predetermined value (Col. 12 lines 51 – 64).

Regarding dependent claim 17, Satagopan et al. further comprising a program

register that stores timing information (TABLE 1 on Col. 11) about when the at least part

of the memory cell array is precharged (Col. 12 lines 51 – 64).

Regarding dependent claim 18, wherein the precharge control circuit (Fig. 7

[Precharge FSM]) causes the memory cell array to be precharged when the timer

reaches (Fig. 7 [720]) a value of the timing information stored in the program register

(TABLE 1 on Col. 11).

Regarding depending claim 19, wherein the program register is a mode

register set (TABLE 1 on Col. 11).

Regarding depending claim 20, wherein the memory device is a DRAM device

(Col. 7 line 24).

Regarding independent claim 21, Fig. 2 of Satagopan et al. discloses a

semiconductor memory device comprising: a plurality of banks (Fig. 3) having a plurality

of memory cells disposed in rows and columns (Fig. 4); a bank selector (Fig. 5 [520]) for

selecting one of the banks in response to an externally received bank address (Fig. 5

[510]), a row selector (Fig. 5 [520]) for selecting one row of the selected bank in

response to an externally received row address (Fig. 5 [510]); a command decoder (Fig.

5 [560]) for decoding a externally received command and activating an auto-precharge

control signal when the decoded command has an auto-precharge function (Col. 10

lines 43 – 58) and a precharge control circuit (Fig. 7[Precharge FSM]) that includes a

plurality of timers (Fig. 7 [720]) corresponding to the plurality of banks, respectively,

wherein the timer corresponding to the selected bank is reset in response to auto

precharge control signal, and controls the bank to be precharged when the timer

reaches a predetermined value (Col. 12 lines 51 – 64).

Regarding dependent claim 22, Satagopan et al. further comprising a program

register that stores timing information regarding when the selected bank is precharged

(TABLE 1 on Col. 11).

Regarding dependent claim 23, wherein the precharge control circuit causes

the selected bank to be precharged when the timer reaches a value of the timing

information stored in the program register (Col. 12 lines 51 – 64).

Regarding dependent claim 24, wherein the program register is mode register

set (TABLE 1 on Col. 11).

Conclusion

4.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

Sugamoto et al.   U.S. Patent No.: 6,559,669 B2   Date of Patent: May 6, 2003

Wilcox   Pub. No.: US 2003/0189870 A1   Pub. Date: Oct. 9, 2003

Contact Information

5.   Any inquiry concerning this communication from the examiner should be directed

to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact

times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's

supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the receptionist, whose telephone number is (703)

305-3900. The faxed phone number for organization where this application or

proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the

patent Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business

Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen   8/30/2005   ANH PHUNG
                                                           PRIMARY EXAMINER